Appendix A

10/091,934

IBM

On-Chip Transmission Lines for High Speed SiGe Applications: Hardware verification status

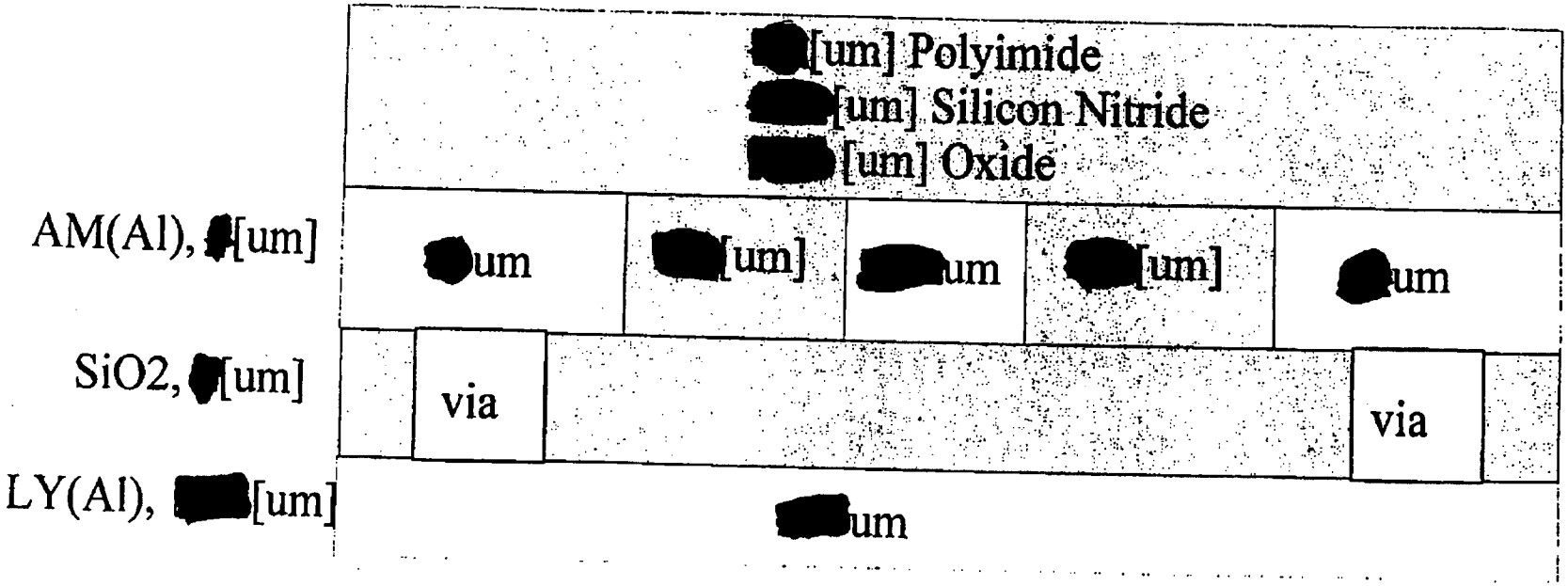
August 2001

Outline

- Studied geometries
- Measurement setup
- EM solver calculation procedure
- IBM T-line model simulation
- SiGe[redacted] technology statistical variation
- Measurement results and EM solver correlation
- Alpha version (January 2001) model vs. measurement
- Beta version (August 2001) model vs. measurement
- Summary & conclusions

Sample No. 1

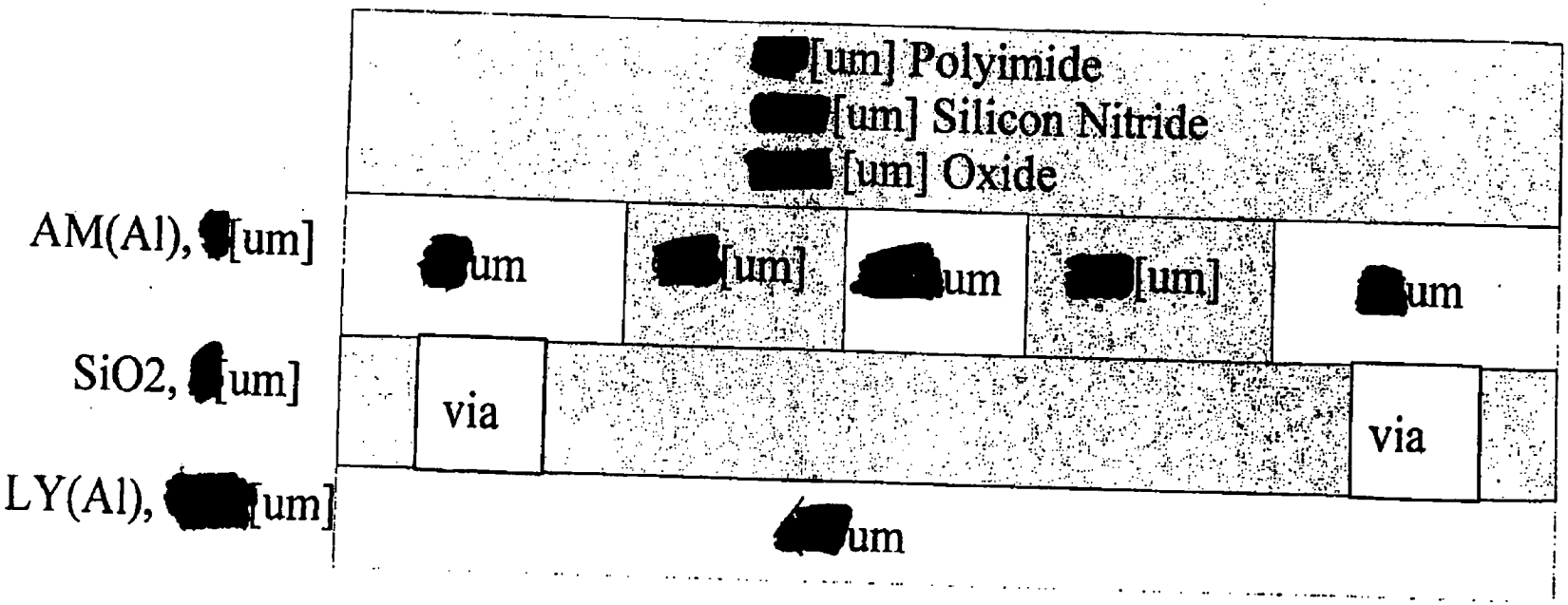
Single ~50 Ohm Transmission Line
Length=1025[um]



probing S/G pad: shielded AM/MT 30[um]X50[um]
Vias present only at both ends of T-line

Sample No. 2

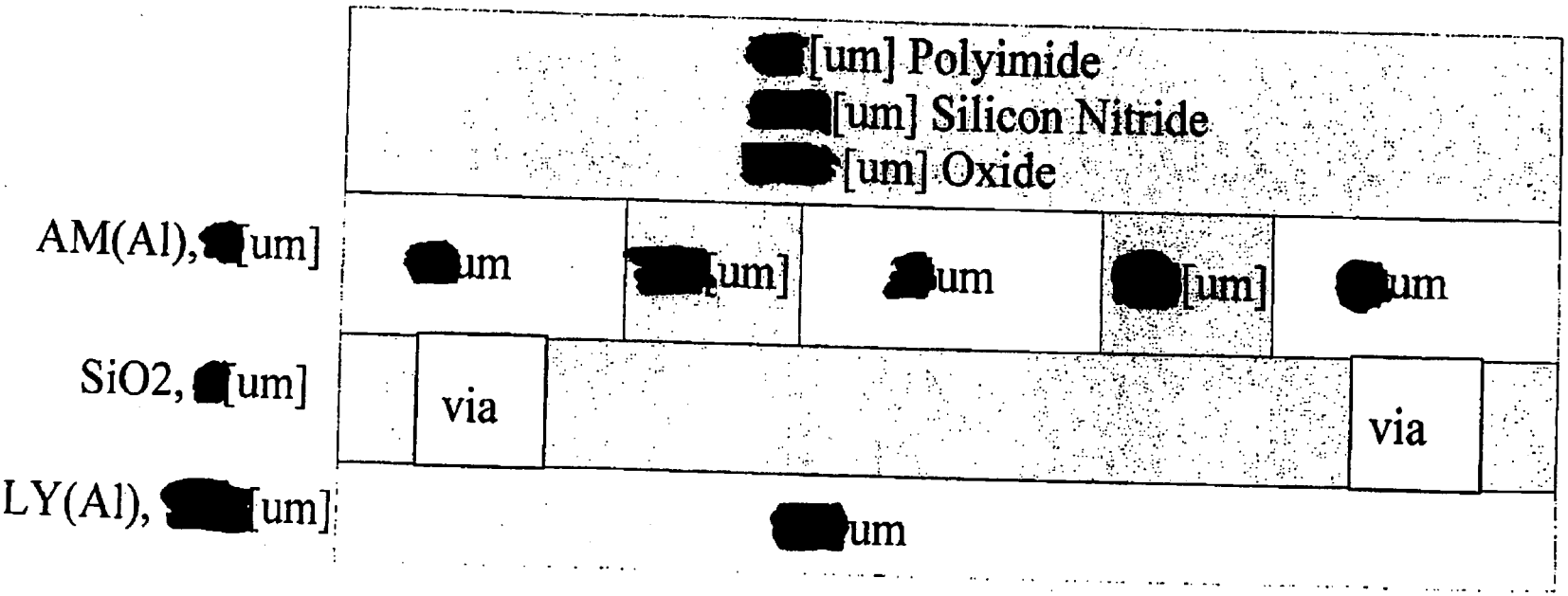
Single ~50 Ohm Transmission Line
Length=4010[um]



probing S/G pad: shielded AM/MT 30[um]X50[um]
Vias present only at both ends of T-line

Sample No. 3

Single ~25 Ohm Transmission Line
Length=4010[um]



probing S/G pad: shielded AM/MT 30[um]X50[um]
Vias present only at both ends of T-line

Hardware measurement setup

- Two port measurement by 8510C Agilent 40[GHz] Vector Network Analyzer.
- Standard 40[GHz] RF coaxial cables.
- Wafer probes: [redacted] coplanar probes, GSG structure, beryllium copper tips (properly cleaned).
- Calibration procedure:
  - LRRM type, using WinCal software.
  - Cascade standard Alumina calibration substrate.
  - On chip de-embedding by open pad structure, and Y-Parameter subtraction.
  - Calibration error: residual tip inductance ~ 10[pH], contact resistance ~ 0.1[Ohm], residual pad capacitance ~5[fF].

EM solver calculation procedure

- Start from Ansoft SI2D quasistatic 2D solver
  (cross sectional dimensions are ~ 0.1% of 40[GHz] equivalent wavelength)
- Impedance mode calculates EM fields inside the metals (full eddy current solution).
- Verify RLC static limits accuracy using Ansoft EM2D.
- Verify asymptotic inductance values (Linfinity) from basic physics relations.
- Perform mathematical conversion to 50[Ohm] based S - Parameters data.
- Verified against HFSS (with solve in metal option). Zero order interpolation (and patience...) is required with HFSS at the low frequency range.

IBM T-line model simulation

- IBM T-line models were simulated in [redacted] environment using the SPECTRES simulator.
- Simulation in S-Parameter mode.
- Two port simulation, with ideal 50[Ohm] ports.
- For the 4[mm] lines, four 1[mm] T-line models were connected in cascade.
- S-parameter data exported directly from SPECTRES and plotted versus the measured data.

SiGe[redacted] technology statistical variation

Based on SiGe[redacted] Design Manual data:

- Metal Line width, Metal line thickness, and SiO_2 dielectric thickness combined variations lead to ~$\pm$10% error in T-line capacitance and T-line inductance values (chip to chip variation).
- Same reasons lead to ~$\pm$10% error in T-line impedance values (chip to chip).
- T-line resistance variation is ~$\pm$20% (chip to chip).

Hardware vs. Solver: Sample 1

Z_0 ~ 50 [Ohm], Length ~ 1[mm]

Magnitude [db]

Phase[degrees]

S11

S12

40[GHz]

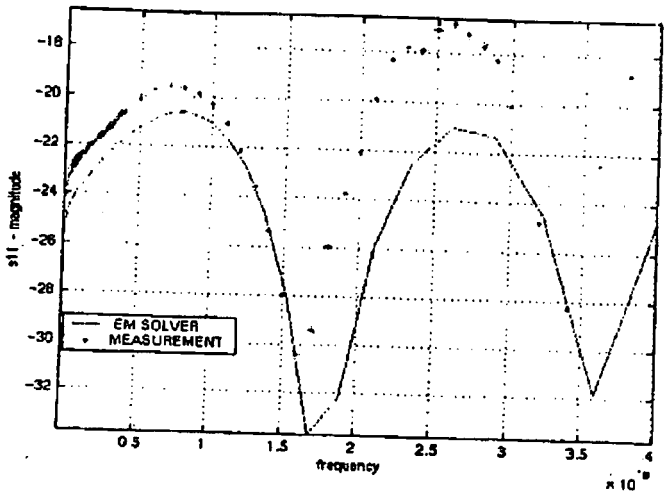
Hardware vs. Solver: Sample 2

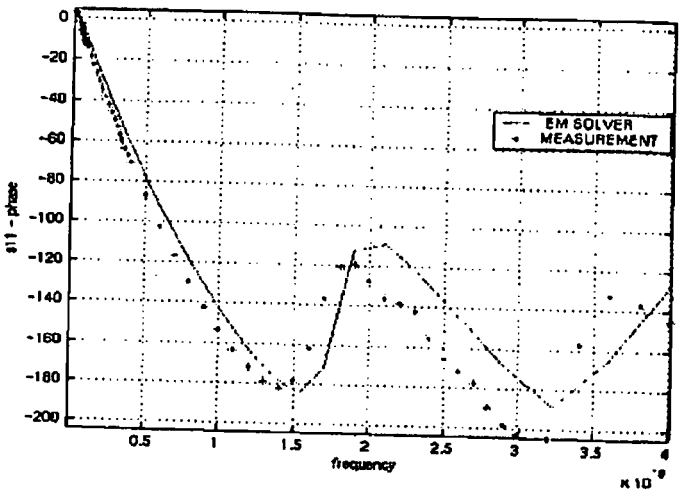
Zo ~ 50 [Ohm], Length ~ 4[mm]

Magnitude [db]

Phase[degrees]

S_{11}

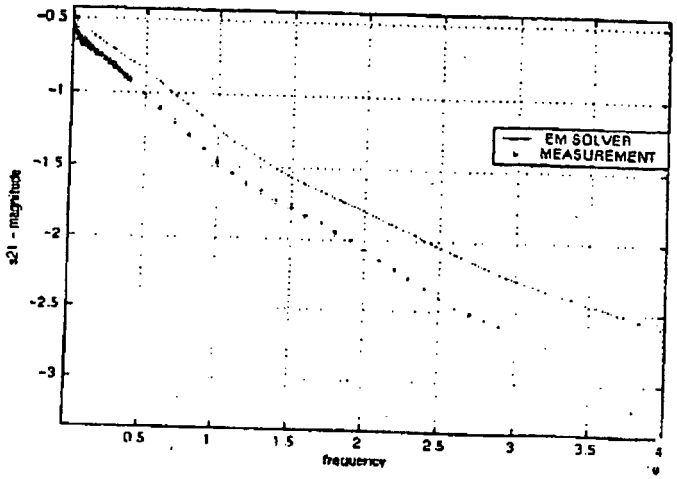


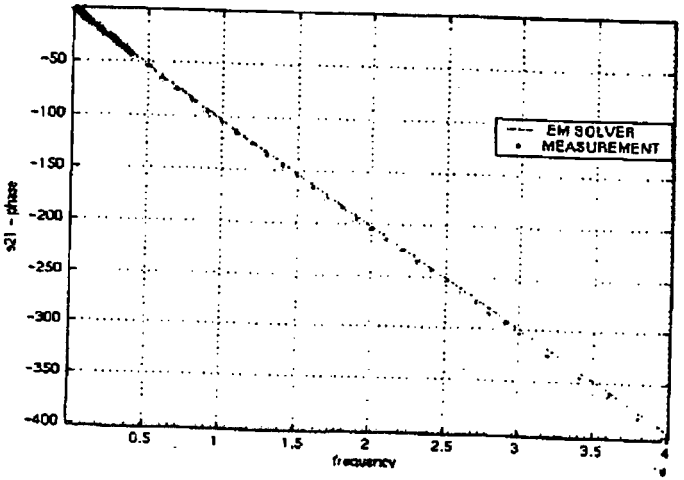


40[GHz]

40[GHz]

S_{12}





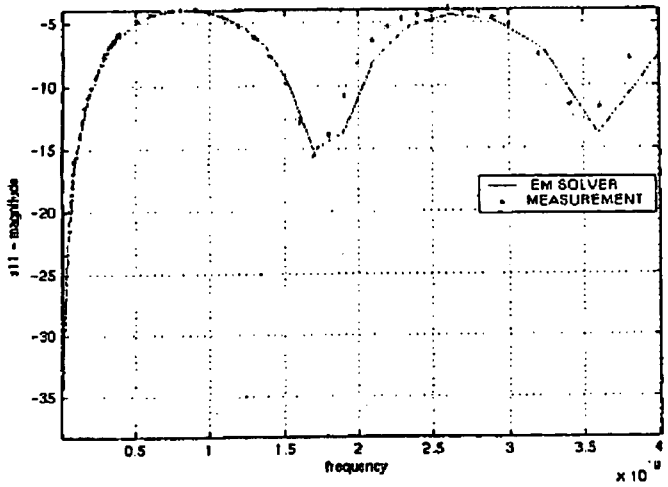
Hardware vs. Solver: Sample 3

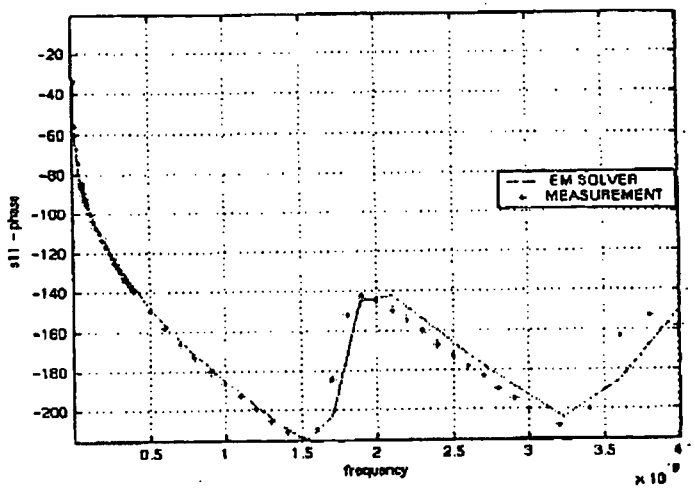
Zo ~ 25 [Ohm], Length ~ 4[mm]

Magnitude [db]

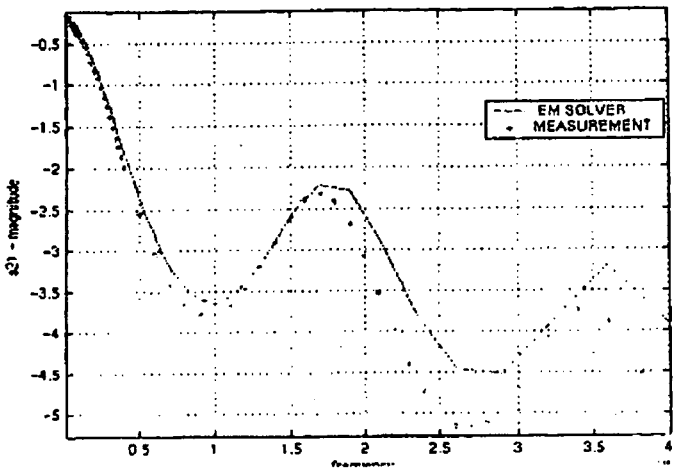
Phase[degrees]

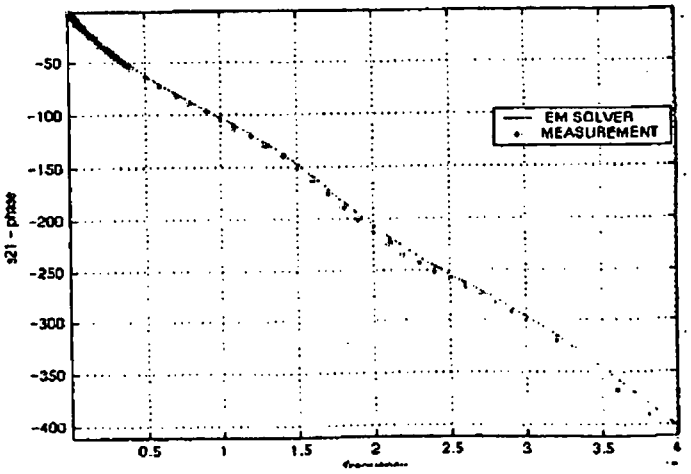
S11





S12





12

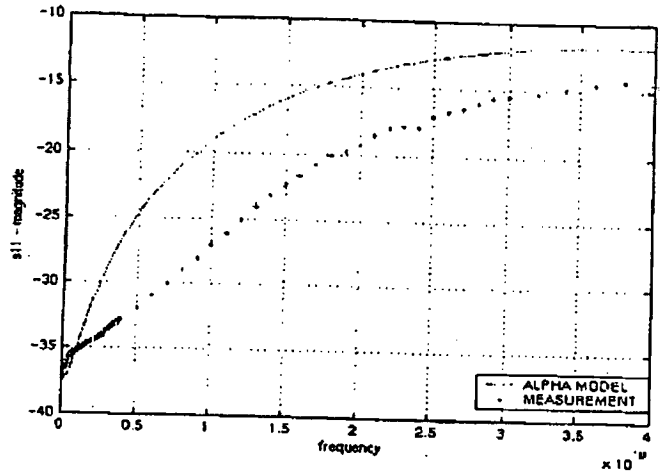
Alpha version results: Sample 1

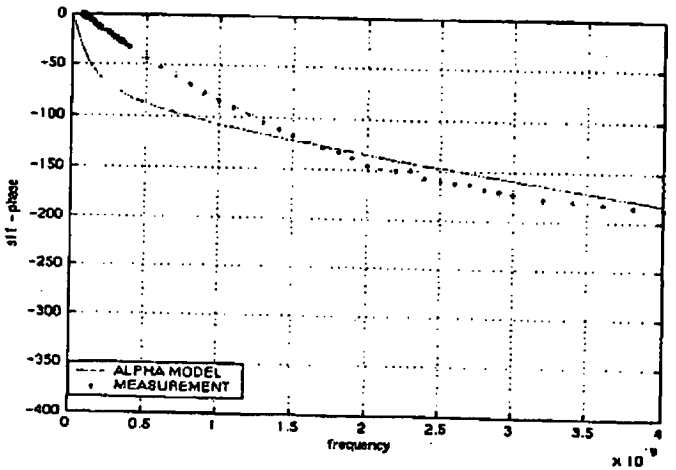
Zo ~ 50 [Ohm], Length ~ 1[mm]

Magnitude [db]

Phase[degrees]

S_{11}

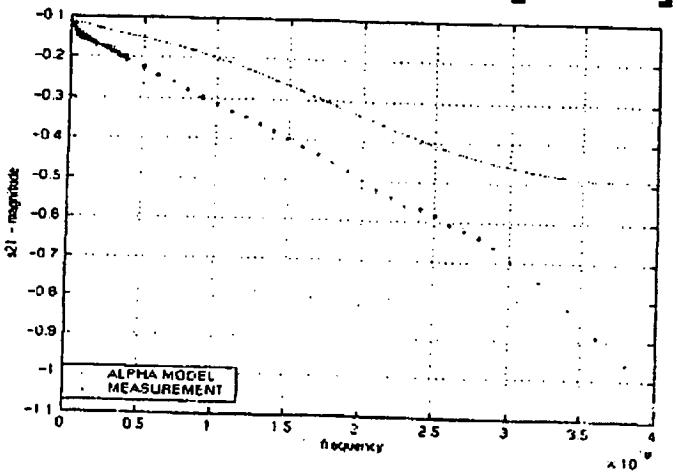


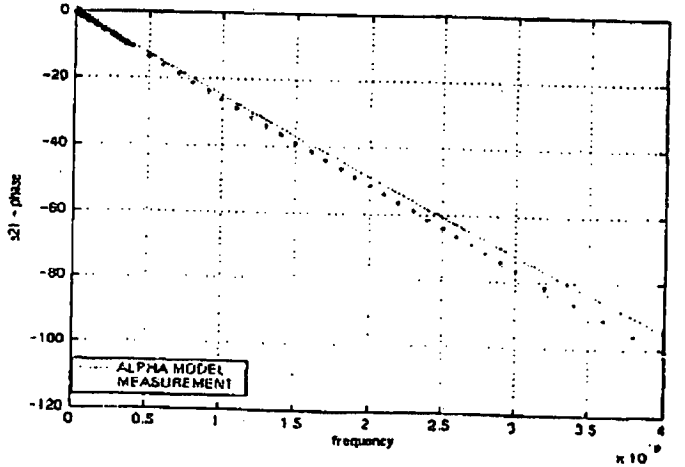


40[GHz]

40[GHz]

S_{12}





13

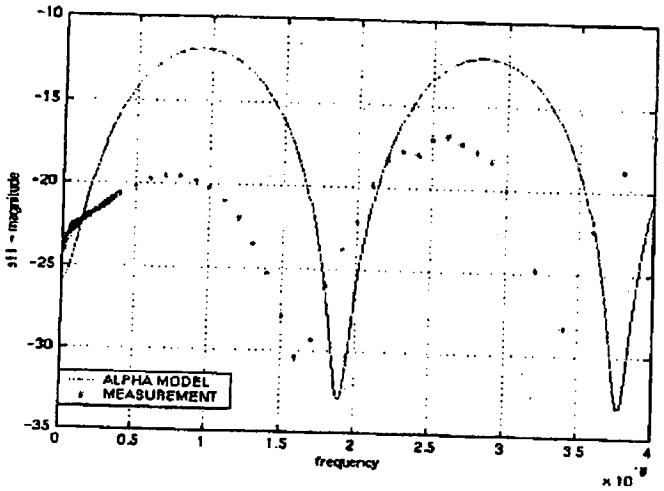
Alpha version results: Sample 2

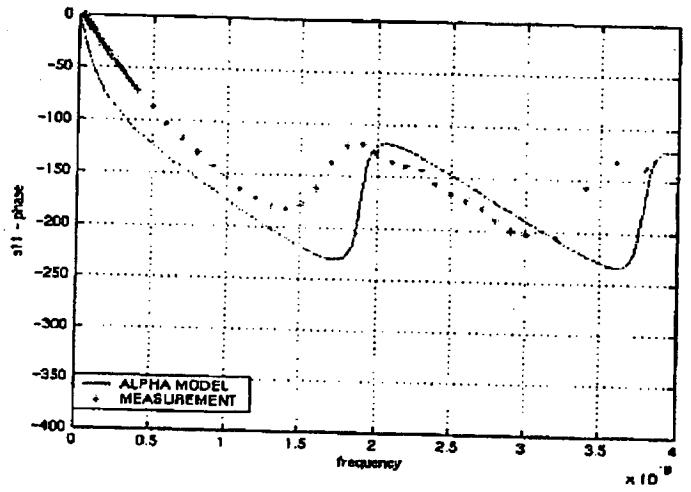
Zo ~ 50 [Ohm], Length ~ 4[mm]

Magnitude [db]

Phase[degrees]

S11

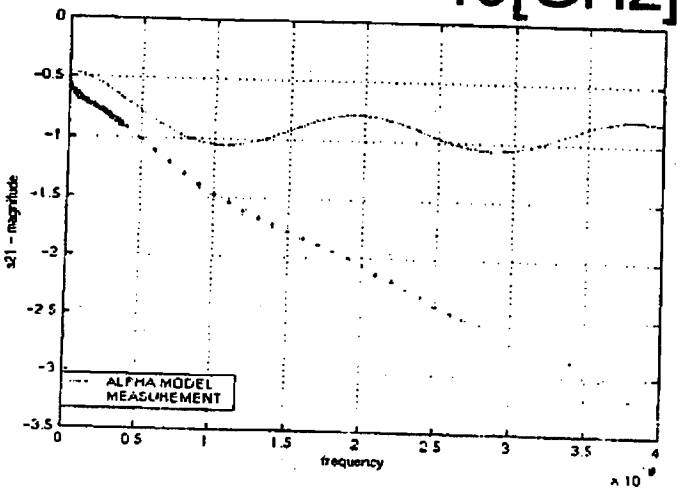


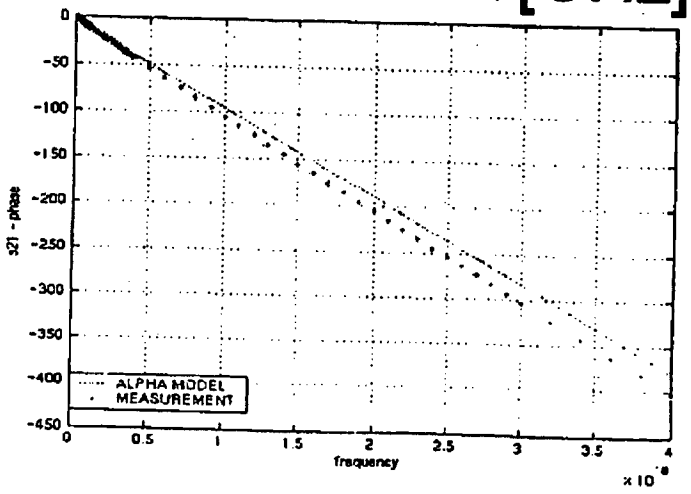


40[GHz]

40[GHz]

S12





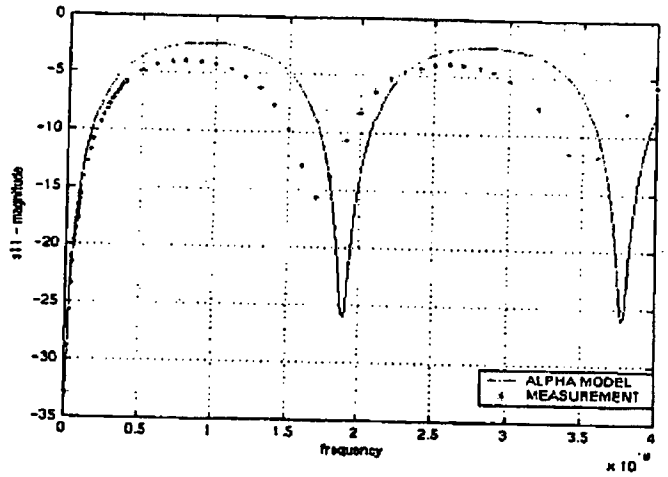
Alpha version results: Sample 3

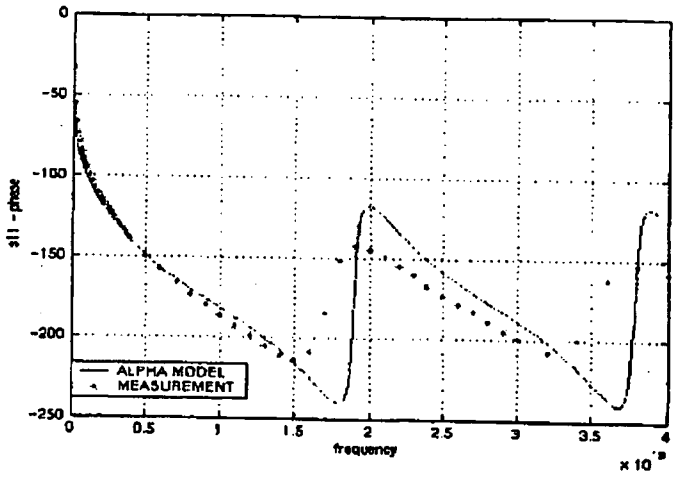
Zo ~ 25 [Ohm], Length ~ 4[mm]

Magnitude [db]

Phase[degrees]

S_{11}

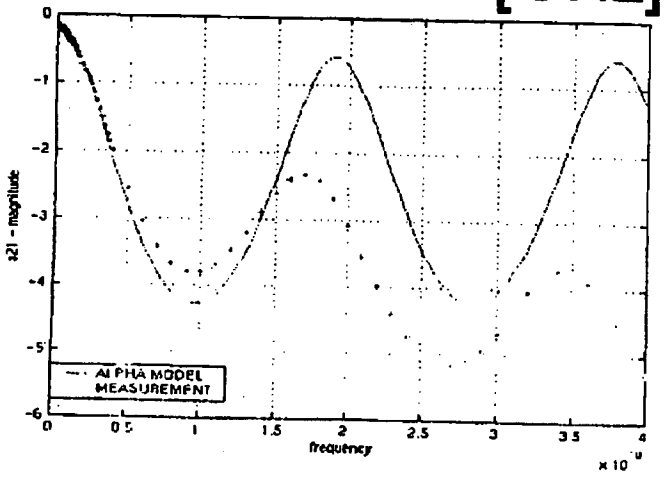


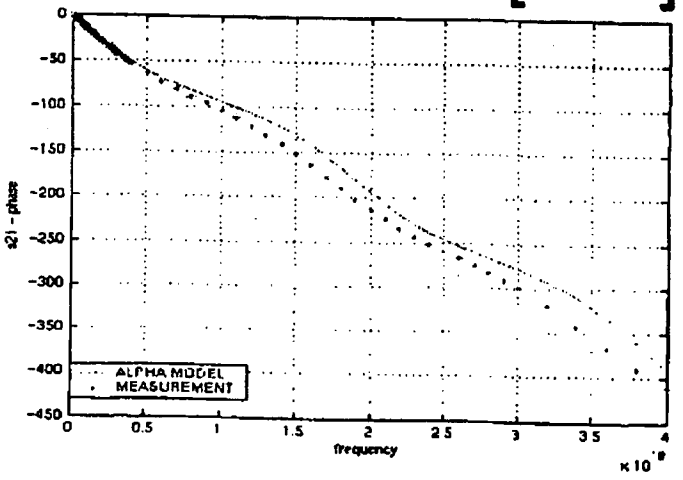


40[GHz]

40[GHz]

S_{12}



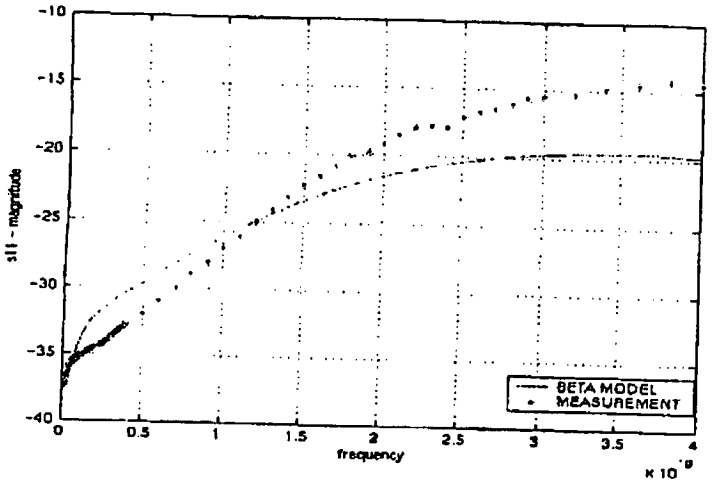


15

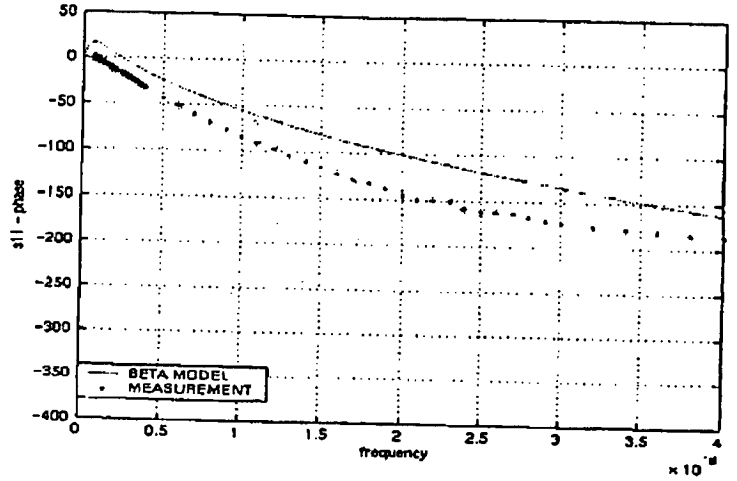
Beta version results: Sample 1

Zo ~ 50 [Ohm], Length ~ 1[mm]

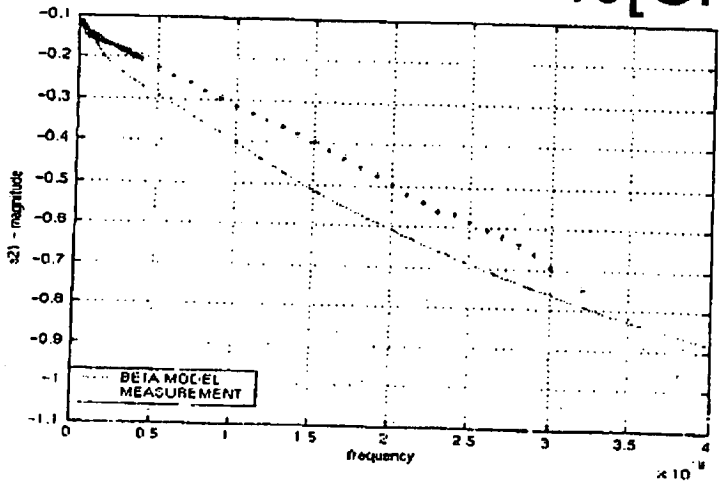
Magnitude [db]



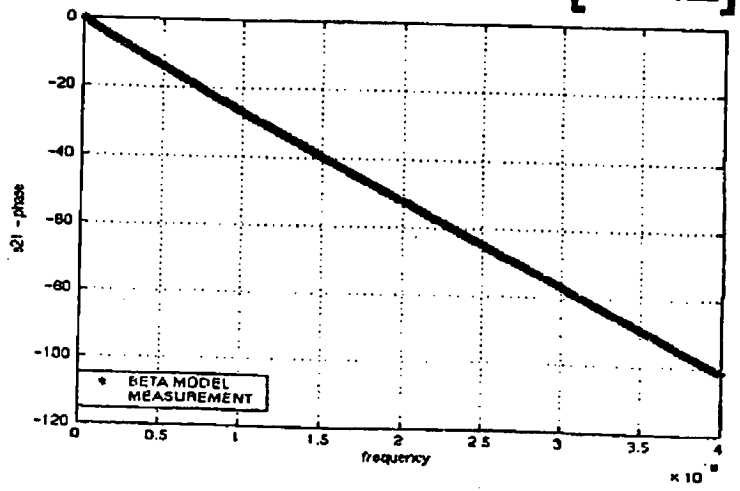
Phase[degrees]



40[GHz]



40[GHz]



16

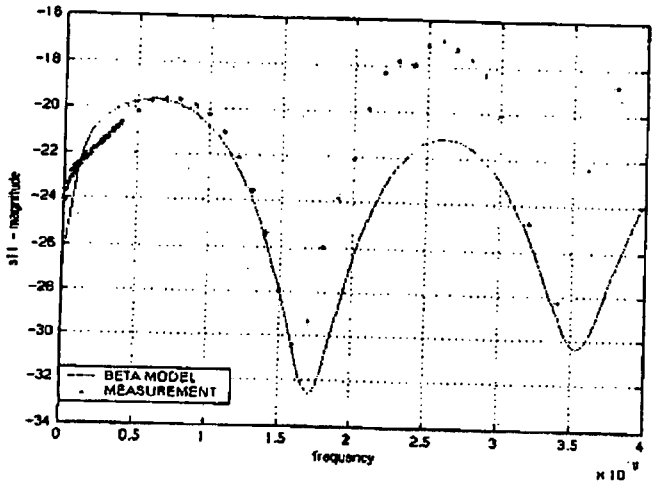
Beta version results: Sample 2

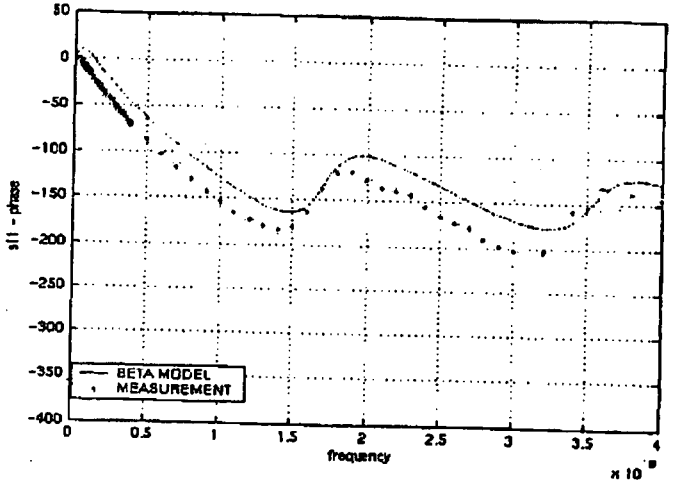
Zo ~ 50 [Ohm], Length ~ 4[mm]

Magnitude [db]

Phase[degrees]

S_{11}

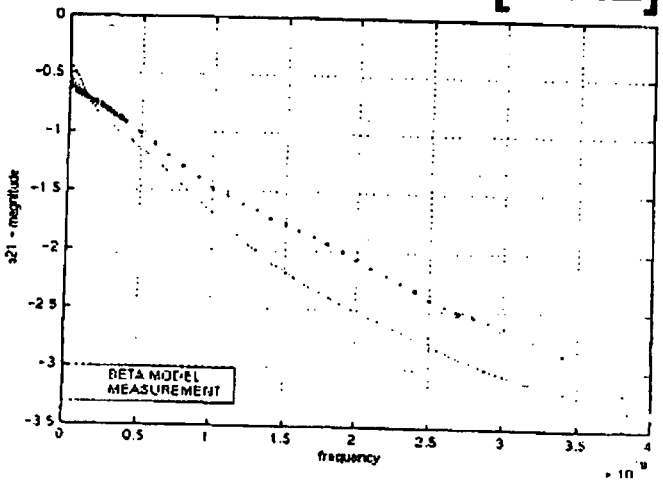


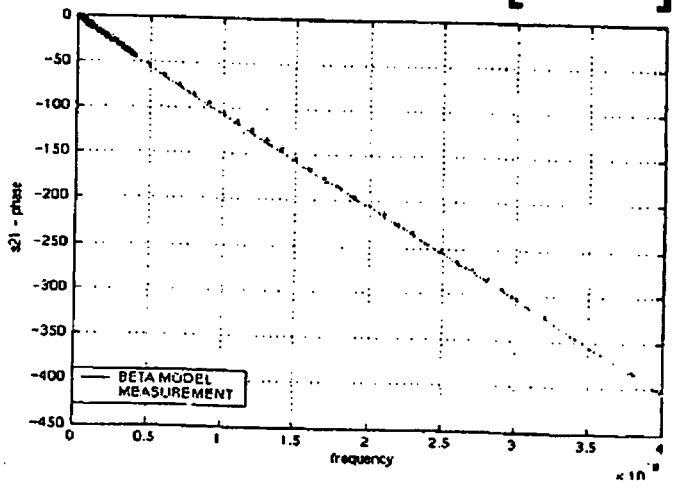


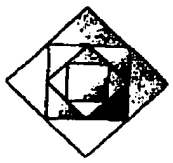
40[GHz]

40[GHz]

S_{12}







Beta version results: Sample 3

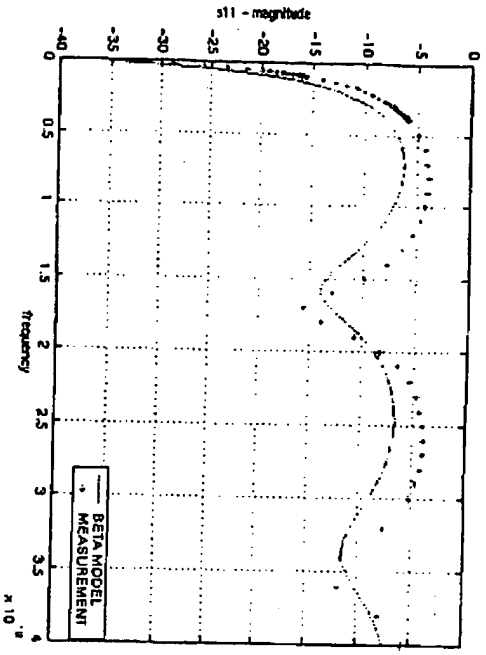
Zo ~ 25 [Ohm], Length ~ 4[mm]

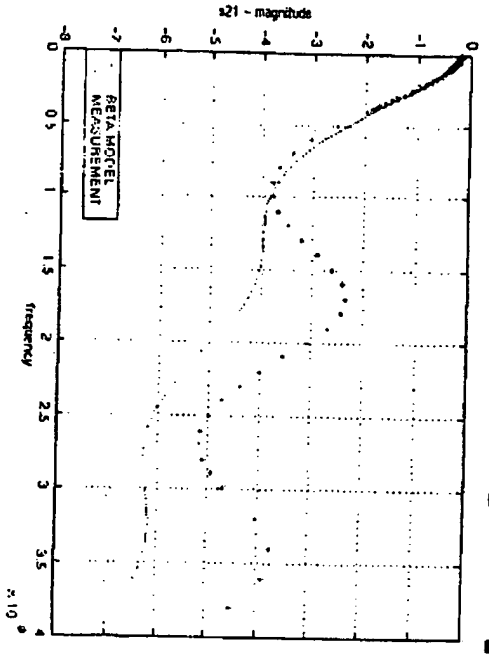
Magnitude [db]

Phase[degrees]

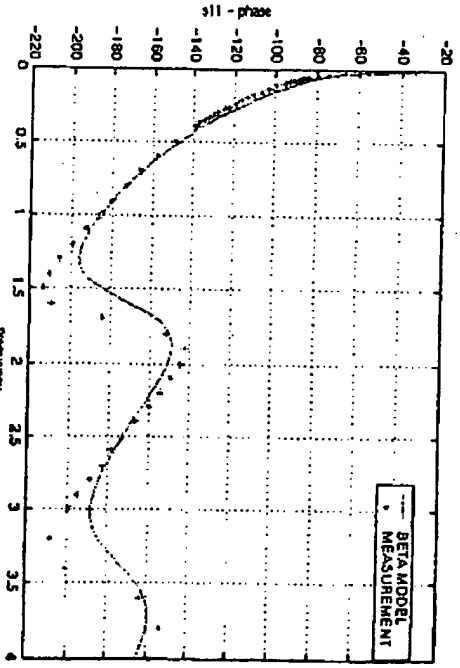
S11

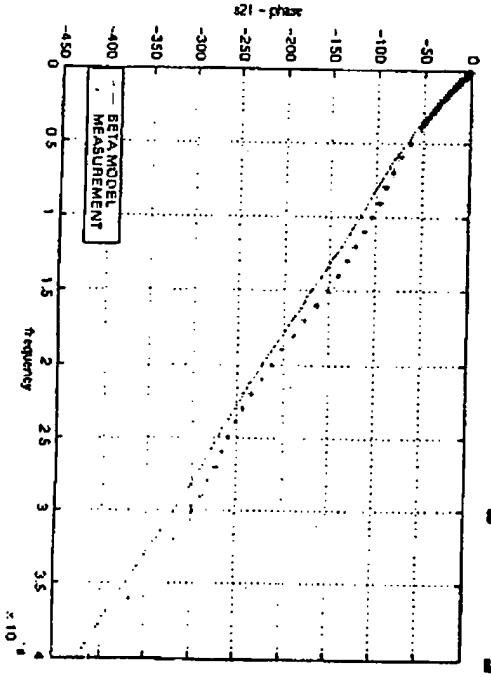
S12





40[GHz]





40[GHz]

12